What is claimed is:

1. A test chip, comprising:

at least one level having an m x n array of regions, where m and n are integers, each region capable of including at least one test structure, at least some of the regions including respective test structures,

the level having m+1 driver lines oriented in a first direction, the m+1 driver lines connected to collectively provide input signals to all of the test structures,

the level having 4n receiver lines arranged in a second direction, the 4n receiver lines connected to collectively receive output signals from all of the test structures,

wherein the test structures are arranged and connected so that each of the structures can be individually addressed for testing using the m+1 driver lines and 4n receiver lines.

2. The test chip of claim 1, wherein:

each test structure is connected to at least one of the driver lines with a first diode, transistor or controlled switch therebetween, and

each test structure is connected to at least one of the receiver lines with a second diode, transistor or controlled switch therebetween.

3. The test chip of claim 1, wherein:

each test structure has two inputs connected by respective diodes, transistors or controlled switches to a respective two of the driver lines, and

each test structure has two outputs connected by respective diodes, transistors or controlled switches to a respective two of the receiver lines.

4. The test chip of claim 1, wherein:

the test structures are arranged in m columns and n rows,

each column has a first one of the driver lines adjacent thereto and connected thereto on a first side thereof and a second one of the driver lines adjacent thereto and connected thereto on a second side thereof,

each row has a first pair of the receiver lines adjacent thereto and connected thereto on a first side thereof and a second pair of the receiver lines adjacent thereto and connected thereto on a second side thereof.

5. The test chip of claim 1, wherein:

the test structures are arranged in n columns and m rows,

each row has a first one of the driver lines adjacent thereto and connected thereto on a first side thereof and a second one of the driver lines adjacent thereto and connected thereto on a second side thereof,

each column has a first pair of the receiver lines adjacent thereto and connected thereto on a first side thereof and a second pair of the receiver lines adjacent thereto and connected thereto on a second side thereof.

6. The test chip of claim 1, wherein:

the test chip has p levels with test structures, where p is an integer greater than one, each of the p levels having m x n regions, at least some of the regions in each level containing test structures,

the chip has p x (m+1) driver lines, with each test structure connected to a respective at least one of the driver lines,

the chip has 8n receiver lines, with each test structure connected to a respective at least one of the receiver lines,

wherein the test structures are arranged and connected so that each of the p x (m x n) test structures can be individually addressed for testing using the p x (m+1) driver lines and 8n receiver lines.

7. The test chip of claim 6, wherein:

the p levels include odd numbered levels and even numbered levels,

each level has 4n receiver lines,

the respective commonly positioned receiver lines from each of the odd numbered levels are connected to each other, and

the respective commonly positioned receiver lines from each of the even numbered levels are connected to each other.

8. A test chip, comprising:

at least one level having an array of regions, each region capable of including at least one test structure, at least some of the regions including respective test structures,

the level having a plurality of driver lines that provide input signals to the test structures,

the level having a plurality of receiver lines that receive output signals from the test structures,

the level having a plurality of devices for controlling current flow,

wherein each test structure is connected to at least one of the driver lines with a first one of the devices therebetween, and

each test structure is connected to at least one of the receiver lines with a second one of the devices therebetween, so that each of the test structures can be individually addressed for testing using the driver lines and receiver lines.

9. The test chip of claim 8, wherein:

each test structure has two inputs connected by respective devices to a respective two of the driver lines, and the devices are from the group consisting of diodes, transistors and controlled switches, and

each test structure has two outputs connected by respective devices to a respective two of the receiver lines, and the devices are from the group consisting of diodes, transistors and controlled switches.

10. The test chip of claim 8, wherein:

the test structures are arranged in m columns and n rows,

each column has a first one of the driver lines adjacent thereto and connected thereto on a first side thereof and a second one of the driver lines adjacent thereto and connected thereto on a second side thereof,

each row has a first pair of the receiver lines adjacent thereto and connected thereto on a first side thereof and a second pair of the receiver lines adjacent thereto and connected thereto on a second side thereof.

11. The test chip of claim 8, wherein:

the test structures are arranged in n columns and m rows,

each row has a first one of the driver lines adjacent thereto and connected thereto on a first side thereof and a second one of the driver lines adjacent thereto and connected thereto on a second side thereof,

each column has a first pair of the receiver lines adjacent thereto and connected thereto on a first side thereof and a second pair of the receiver lines adjacent thereto and connected thereto on a second side thereof.

12. The test chip of claim 8, wherein:

the test chip has p levels with test structures, where p is an integer greater than one, each of the p levels having regions, at least some of the regions in each level containing test structures, the p levels include odd numbered levels and even numbered levels,

each level has commonly positioned receiver lines,

the respective commonly positioned receiver lines from each of the odd numbered levels are connected to each other, and

the respective commonly positioned receiver lines from each of the even numbered levels are connected to each other.

13. A test chip, comprising:

at least one level having an array of regions with m columns and n rows, where m and n are integers, each region capable of including at least one test structure, at least some of the regions including respective test structures,

the level having m+1 driver lines oriented in a first direction, with the m columns arranged between successive ones of the m+1 driver lines, each test structure having two inputs connected by respective diodes, transistors, or controlled switches to a respective two of the driver lines, the m+1 driver lines collectively providing input signals to all of the test structures,

the level having 4n receiver lines oriented in a second direction, each of the n rows arranged between a respective first pair of the 4n receiver lines on a first side thereof and a respective second pair of the 4n receiver lines on a second side thereof, each test structure having first and second outputs connected by respective diodes, transistors or controlled switches to respective ones of the receiver lines on the first and second side of that test structure, so that the 4n receiver lines collectively receive output signals from all of the test structures, whereby each of the structures can be individually addressed for testing.

14. The test chip of claim 13, wherein:

the test chip has p levels with test structures, where p is an integer greater than one, each of the p levels having m x n regions, at least some of the regions in each level containing test structures,

the chip has p x (m+1) driver lines, with each test structure connected to a respective at least one of the driver lines,

the chip has 8n receiver lines, with each test structure connected to a respective at least one of the receiver lines,

wherein the test structures are arranged and connected so that each of the p x (m x n) test structures can be individually addressed for testing using the p x (m+1) driver lines and 8n receiver lines.

15. The test chip of claim 14, wherein:

the p levels include odd numbered levels and even numbered levels,

each level has 4n receiver lines,

the respective commonly positioned receiver lines from each of the odd numbered levels are connected to each other, and

the respective commonly positioned receiver lines from each of the even numbered levels are connected to each other.

16. A test chip, comprising:

at least one layer having n regions, where n an integer, each region capable of including at least one test structure, at least some of the regions including respective test structures, each comprising a nest of m parallel lines, where m is an integer,

the at least one layer having m driver lines, the m driver lines connected to provide input signals to the respective m parallel lines in each nest,

the at least one layer having at least 2n receiver lines, the at least 2n receiver lines connected to collectively receive output signals from all of the test structures,

wherein the test structures are arranged and connected to the m driver lines and at least 2n receiver lines so that a presence of a short or open circuit defect in any of the nests can be identified.

17. The test chip of claim 16, wherein the layer has 3n receiver lines.

18. The test chip of claim 16, wherein :

the test chip has p layers, each layer having n regions, at least some of the regions in each layer including respective nests of m parallel lines,

each of the p layers having m driver lines, the m driver lines connected to provide input signals to the respective m parallel lines in each nest in that respective layer,

each layer having at least 2n receiver lines, the at least 2n receiver lines connected to collectively receive output signals from all of the test structures in that respective layer.

19. The test chip of claim 18, wherein the receiver lines having corresponding connections in each respective one of the odd numbered layers are connected to each other.

20. The test chip of claim 19, wherein the test structures and receiver lines in the odd numbered layers are oriented in a common direction.

21. The test chip of claim 19, wherein the receiver lines having corresponding connections in each respective one of the even numbered layers are connected to each other.

22. The test chip of claim 21, wherein:

the test structures and receiver lines in the odd numbered layers are oriented in a first common direction; and

the test structures and receiver lines in the even numbered layers are oriented in a second common direction different from the first common direction.

23. A test method, comprising the steps of:

(a) forming circuit paths for at least one level of a chip, the level having an m x n array of regions, where m and n are integers, at least some of the regions including respective test structures,

(b) forming m+1 driver lines oriented in a first direction, each test structure being connected to at least one of the driver lines;

(c) forming 4n receiver lines arranged in a second direction, each test structure being connected to at least one of the receiver lines;

(d) individually addressing all the test structures using the m+1 driver lines and 4n receiver lines; and

(e) providing input signals to all of the test structures using the m+1 driver lines, and

(f) receiving output signals from all of the test structures using the 4n receiver lines.

24. The test method of claim 23, wherein:

each test structure has two inputs connected by respective diodes, transistors or controlled switches to a respective two of the driver lines, and

each test structure has two outputs connected by respective diodes, transistors or controlled switches to a respective two of the receiver lines.

25. The method of claim 23, wherein:

each test structure in the level is connected to at least one of the driver lines with a first diode therebetween,

each test structure in the level is connected to at least one of the receiver lines with a second diode therebetween,

step (e) includes performing as one of the group consisting of an inner loop and an outer loop a sequence of successively applying a first signal to each driver line of the level, one at a time, while applying a second signal to all remaining driver lines in the level; and

step (f) includes performing as the other of the group consisting of the inner loop and the outer loop a sequence of measuring a current to ground at each receiver line of the level, wherein the inner loop is performed each time the an iteration of the outer loop is performed.

26. The method of claim 23, wherein:

each test structure in the level is connected to at least one of the driver lines with a first transistor therebetween,

each test structure in the level is connected to at least one of the receiver lines with a second transistor therebetween, and

step (e) includes performing as one of the group consisting of an inner loop and an outer loop a sequence of successively applying a first voltage to each driver line of the level, one at a time, while applying a second voltage to all remaining driver lines in the level;

step (f) includes performing as the other of the group consisting of the inner loop and the outer loop a sequence of applying the second voltage to each receiver line of the level, one at a time, while applying the first voltage to all remaining receiver lines in the level; and

the method further comprises measuring a wafer substrate current to ground each time the second voltage is applied to a different receiver line in step (e).

27. The test method of claim 23, wherein:

the chip has p levels with test structures, where p is an integer greater than one, each of the p levels having m x n regions, at least some of the regions in each level containing test structures,

the chip has p x (m+1) driver lines, with each test structure connected to a respective at least one of the driver lines,

the chip has 8n receiver lines, with each test structure connected to a respective at least one of the receiver lines, and

step (d) includes individually addressing the p x (m x n) test structures for testing using the p x (m+1) driver lines and 8n receiver lines.

28. The test method of claim 27, wherein:

the p levels include odd numbered levels and even numbered levels,

each level has 4n receiver lines,

and the method further comprises:

connecting the respective commonly positioned receiver lines from each of the odd numbered levels to each other, and

connecting the respective commonly positioned receiver lines from each of the even numbered levels to each other.

29. A test method, comprising the steps of:

(a) forming circuit paths for at least one layer having n regions, where n is an integer, each region capable of including at least one test structure, at least some of the regions including respective test structures, each comprising a nest of m parallel lines, where m is an integer,

(b) forming m driver lines for the at least one layer;

(c) forming at least 2n receiver lines for the at least one layer;

(d) providing input signals to the respective m parallel lines in each nest using the m driver lines;

(e) measuring output signals from all of the test structures using the at least 2n receiver lines; and

(f) identifying the presence of a short or open circuit defect in any of the nests based on the output signals received by way of the at least 2n receiver lines.

30. The test method of claim 29, wherein the layer has 3n receiver lines, and step (f) includes identifying the presence of a short or open circuit defect in any of the nests based on the output signals received by way of the 3n receiver lines.

31. The test method of claim 29, wherein :

the test chip has p layers, each layer having n regions, at least some of the regions in each layer including respective nests of m parallel lines,

each of the p layers having m driver lines, the m driver lines connected to provide input signals to the respective m parallel lines in each nest in that respective layer,

each layer having at least 2n receiver lines, the at least 2n receiver lines connected to collectively receive output signals from all of the test structures in that respective layer.

32. The test method of claim 31, further comprising connecting receiver lines having corresponding positions in each respective one of the odd numbered layers to each other.

33. The test method of claim 32, wherein the test structures and receiver lines in the odd numbered layers are oriented in a common direction.

34. The test method of claim 32, further comprising connecting receiver lines having corresponding positions in each respective one of the even numbered layers to each other.

35. The test method of claim 32, wherein:

the test structures and receiver lines in the odd numbered layers are oriented in a first common direction; and

the test structures and receiver lines in the even numbered layers are oriented in a second common direction different from the first common direction.

36. The test method of claim 29, wherein

each test structure in the layer is connected to at least one of the driver lines with a first transistor therebetween,

each test structure in the layer is connected to at least one of the receiver lines with a second transistor therebetween,

step (d) includes performing as one of the group consisting of an outer loop and an inner loop a sequence of successively applying a first voltage to each driver line of the layer, one at a time, while applying a second voltage to all remaining driver lines in the layer;

step (e) includes performing as the other of the group consisting of the outer loop and the inner loop a sequence of applying the second voltage to each receiver line of the layer, one at a time, while applying the first voltage to all remaining receiver lines in the layer; and

the method further comprises measuring a wafer substrate current to ground each time the second voltage is applied to a different receiver line in step (e).

37. The method of claim 29, wherein:

each test structure in the layer is connected to at least one of the driver lines with a first diode therebetween,

each test structure in the layer is connected to at least one of the receiver lines with a second diode therebetween,

and step (e) includes

performing as one of the group consisting of an inner loop and an outer loop a step of successively applying a first signal to each driver line of the level, one at a time, while applying a second signal to all remaining driver lines in the level; and

performing as the other of the group consisting of the inner loop and the outer loop a step of measuring a current to ground at each receiver line of the level.

38. A test chip, comprising:

at least one layer having a vector of regions, each region capable of including at least one test structure, at least some of the regions including respective test structures,

the layer having a plurality of driver lines that provide input signals to the test structures,

the layer having a plurality of receiver lines that receive output signals from the test structures,

the layer having a plurality of devices for controlling current flow,

wherein each test structure is connected to at least one of the driver lines with a first one of the devices therebetween, and

each test structure is connected to at least one of the receiver lines with a second one of the devices therebetween, so that each of the test structures can be individually addressed for testing using the driver lines and receiver lines.

1 39. The test chip of claim 1, wherein each test structure has four or fewer pins.

1 40. The test chip of claim 8, wherein each test structure has four or fewer pins.

1 41. The test chip of claim 13, wherein each test structure has four or fewer pins.

1 42. The test chip of claim 16, wherein each test structure has four or fewer pins.